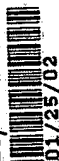


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**U.S. UTILITY Patent Application**

**PATENT NUMBER and  
ISSUE DATE**

APPL NUM 10057024	FILING DATE 01/25/02	CLASS 549	SUBCLASS 5	GAU 1626	EXAMINER Lambkin
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**CONTINUING DATA VERIFIED:**

THIS APPLICATION IS A CONTINUATION OF 09/814,232 07/12/2001 PAT. NO. 6,414,164

**CONTINUING DATA VERIFIED:**

<input type="checkbox"/> YES	<input type="checkbox"/> NO
<input type="checkbox"/> YES	<input type="checkbox"/> NO
<input type="checkbox"/> YES	<input type="checkbox"/> NO

Verbal description of the invention's initials

FIG. 1 is a schematic diagram of a semiconductor device and their interconnection channel in a semiconductor device.

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<b>NOTICE OF ALLOWANCE MAILED</b>		<b>CLAIMS ALLOWED</b>	
		Total Claims	Print Claim for O.G.
<b>ISSUE FEE</b>		<b>DRAWING</b>	
Amount Due	Date Paid	Sheets Drwg.	Figs. Drwg.
		Print Fig.	
<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>		<b>Application Examiner</b>	
		<b>PREPARED FOR ISSUE</b>	
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